

SYSTEM PAGE REF.

PAUSE	COMMENT
001_Misc Diagram	
002_System Setting	
003_CPU DISPLAY	
004_CPU_0043	
005_CPU_LAP-REF,SWR,CLUSE	
006_CPU_0046	
007_CPU_MISC,PTAS	
008_CPU_CPU_0047	
009_CPU_0048	
010_CPU_0049	
011_CPU_0050	
012_CPU_0051	
013_CPU_0052	
014_CPU_0053	
015_CPU_0054	
016_CPU_0055	
017_CPU_0056	
018_CPU_0057	
019_CPU_0058	
020_CPU_0059	
021_CPU_0060	
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023_CPU_0062	
024_CPU_0063	
025_CPU_0064	
026_CPU_0065	
027_CPU_0066	
028_CPU_0067	
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030_CPU_0069	
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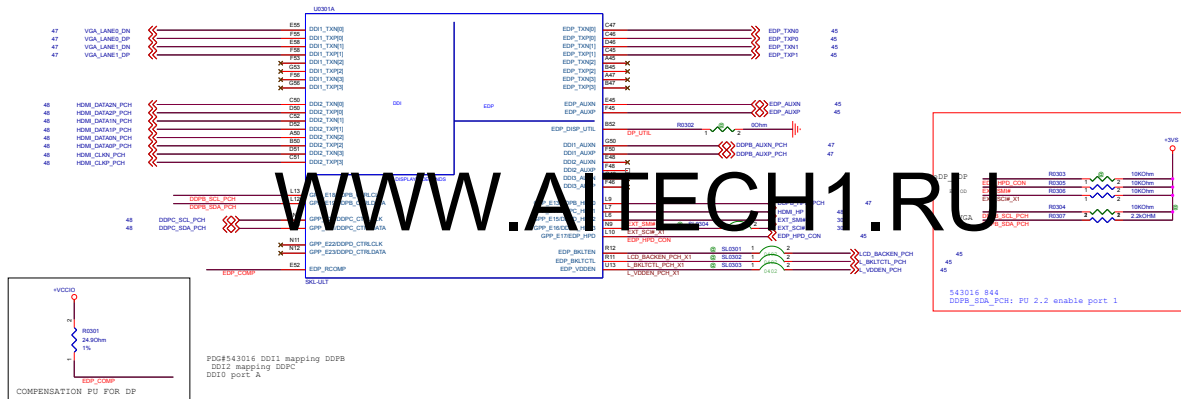
Use as CPO 16/2.
CPO: nothing to
CPO 16/2.

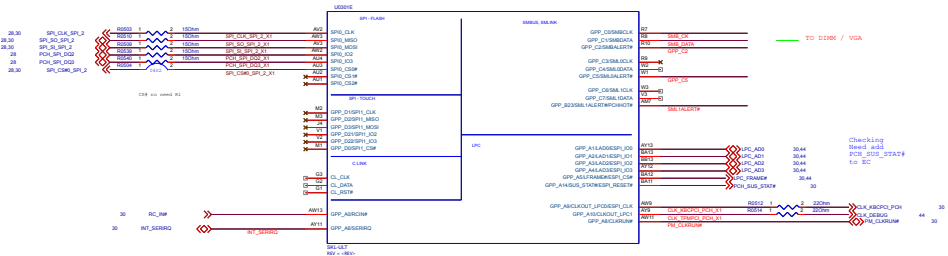
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Display Port

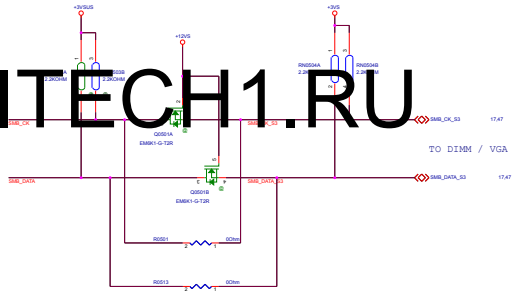
A	EDP
B	VGA
C	HDMI

Intel Version	ASUS P/N

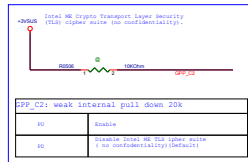
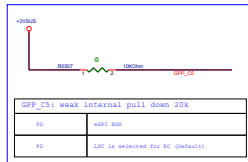


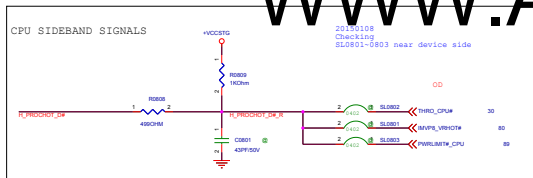
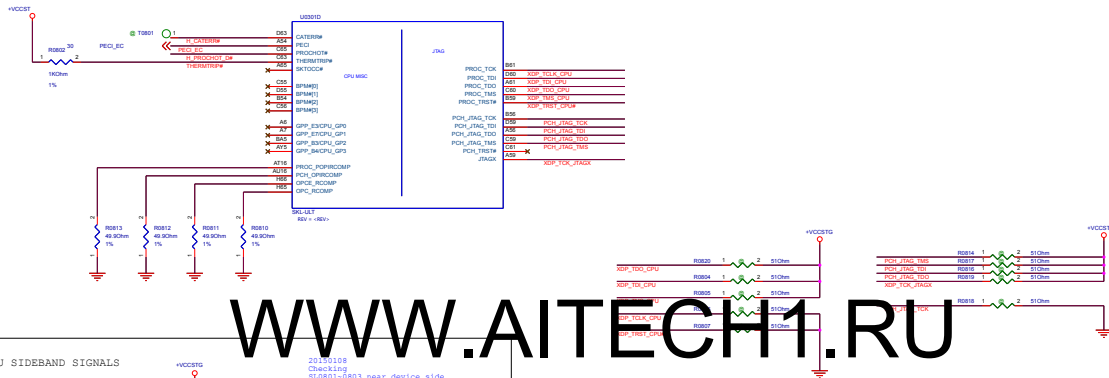


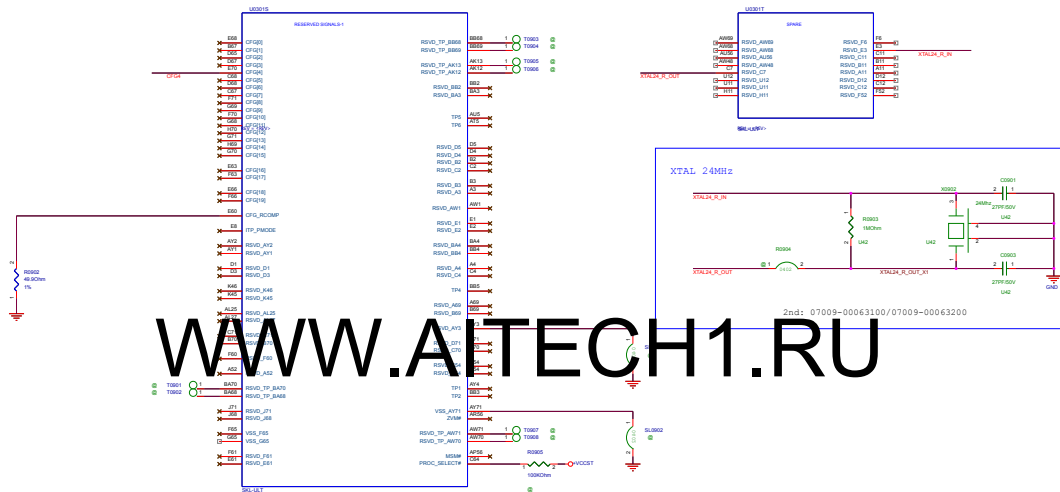
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```
SM11ALERT# /PCHHOT#/GPT_B23
LOW during strap sampling:internal 20K PD;
When used as PCHHOT#, a 150k weak board
pull-up is recommended ;
```





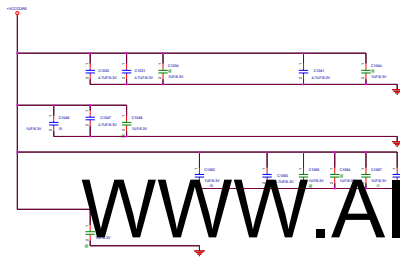


	1	0	NOTE
CFG4	DISABLE	ENABLE	#DP ENABLE

BOM

Project Name		Rev
ASUS X441UBR		R2.1
Title: CPU_CFG.RSVD		
Size	Dept.: ASUS/TAI COMPUTER INC.	Engineer: SZ/EE
Custom		
Date: Friday, April 27, 2018		Sheet 2 of 100

CPU - VCC DECAPS- Underneath the package



Sizeable: C1034, C1044, C1046, C1048, C1062, C1064, C1065, C1067
 1402.4.7uF: C1030, C1031, C1041, C1047, C1043, C1044

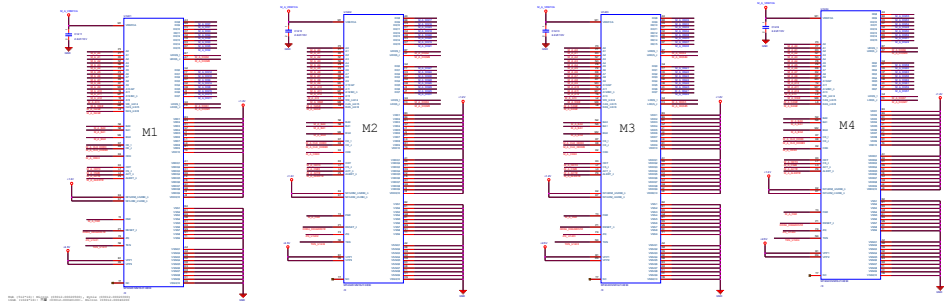
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CPU - VCC DECAPS- Place close to the package

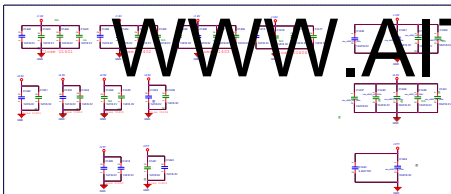
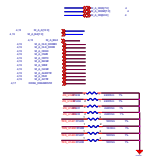
CAP above 220F move to PWB page

Cap options check on

		Project Name		Rev
X4410BR				A01
Title:		CPU_POWER_CAP		
Item	Dept:	ASUSTek COMPUTER INC.		Engineer: S202
C				
Date: Friday, June 27, 2019		Drawn	By	Ref: 102



Reference Designator - Component		
Designator	Component	Value
U1	MAX9845	MAX9845
U2	MAX9845	MAX9845
U3	MAX9845	MAX9845
U4	MAX9845	MAX9845
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U6	MAX9845	MAX9845
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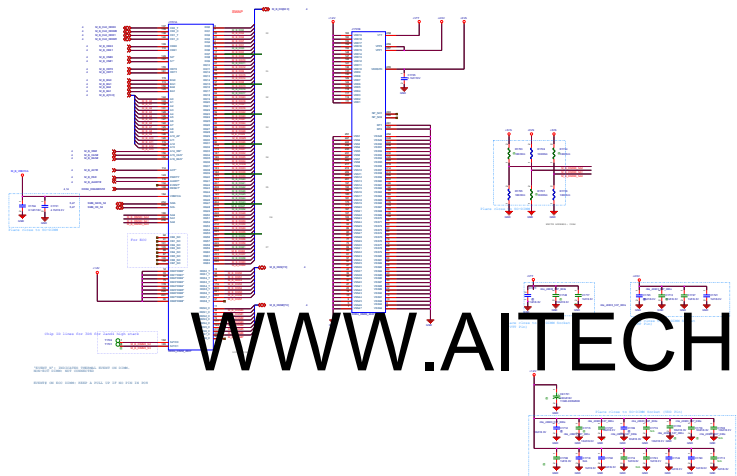
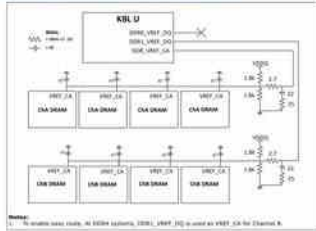


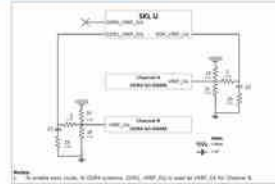
Figure 4-53: KBL U DDR4 x16 Devices Memory Down Vref_CK Overview



Note(s):
1. To enable auto mode, set DDR4_0000_0000_0000_0000 to 0x0000_0000_0000_0000.

All Vref trace must be 20 mils width

Figure 4-54: KBL U DDR4 x16 Devices Memory Down Vref_CK Overview

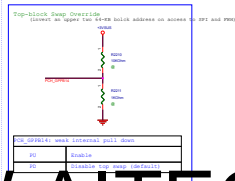
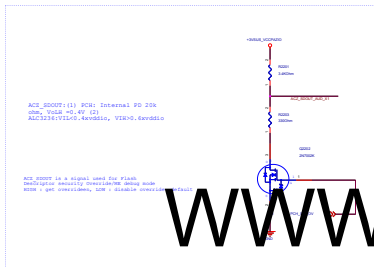
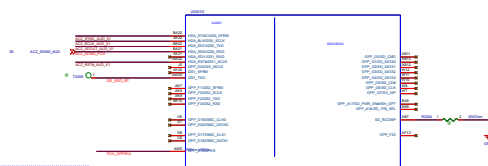


Note(s):
1. To enable auto mode, set DDR4_0000_0000_0000_0000 to 0x0000_0000_0000_0000.



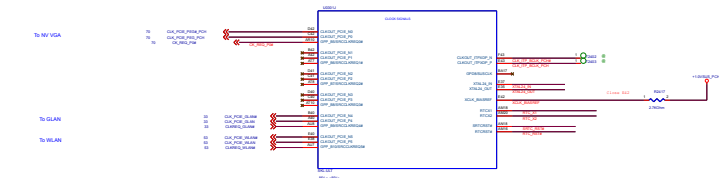




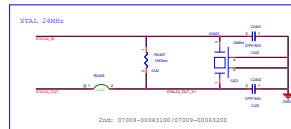
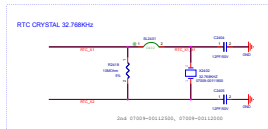


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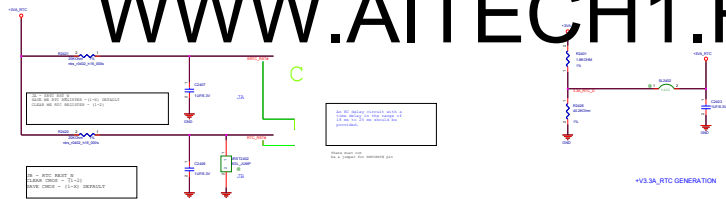
[illegible]



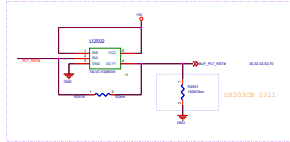
CHECK P0B0 CLK



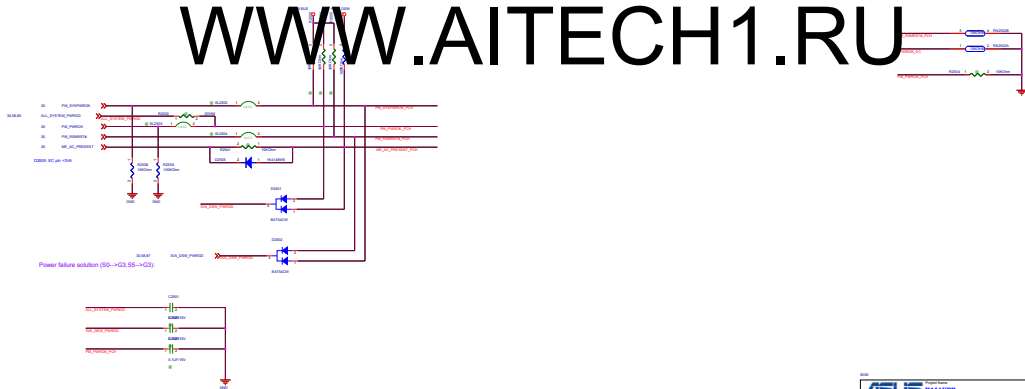
WWW.AITECH1.RU

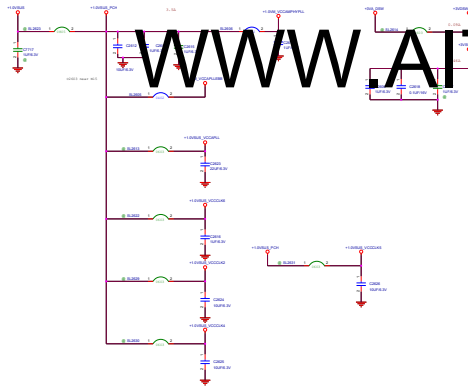
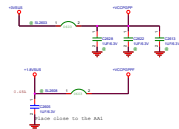
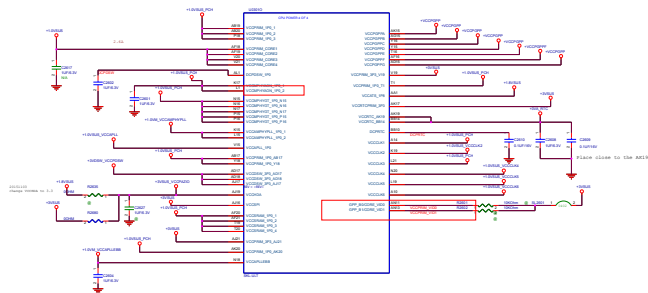


ASUS		Project Name	ASUS
Model		X441UBR	Rev
Title :		CPU_FCH_CLOCK_SIGNALS.HTC	Rev
Rev	Dept. : ASUS/TA COMPUTER INC. Engineer :		EE
Date	Friday, April 27, 2018		Sheet 24 of 103



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WWW.AITECH1.RU

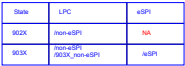
$$REV = \langle REV \rangle$$
$$\overline{REV} = \langle REV \rangle$$

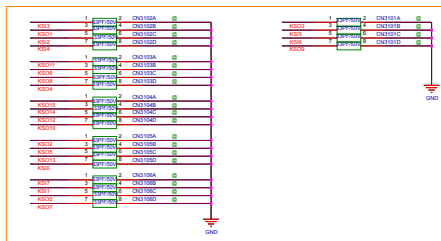
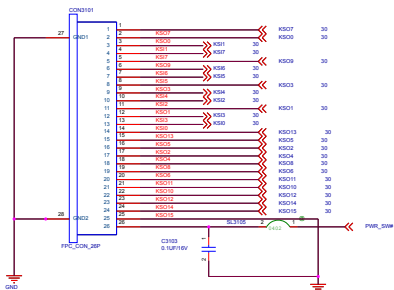
BOM

Rev	 Project Name X441UBR	Rev R2.1
Title : CPU_PCH_POEWR,GND		
Size B	Dept.: ASUSTek COMPUTER INC	Engineer: EE
Date: Friday, April 27, 2018	Sheet 27	of 102



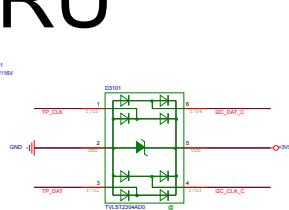
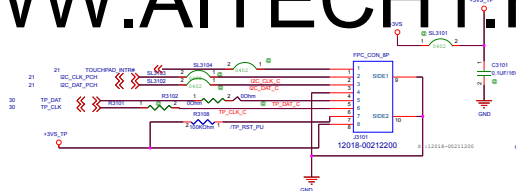
ASUS		Project Name		No.	
		X441UBR		R4	
Title :		PCH-SPI ROM,OTH			
Size	Dept. :		ASUS&w.COMPUTER INC.		Engineer: EE
A3					
Date: Friday April 27, 2018		Sheet		28	of 102






WWW.AITECH1.RU

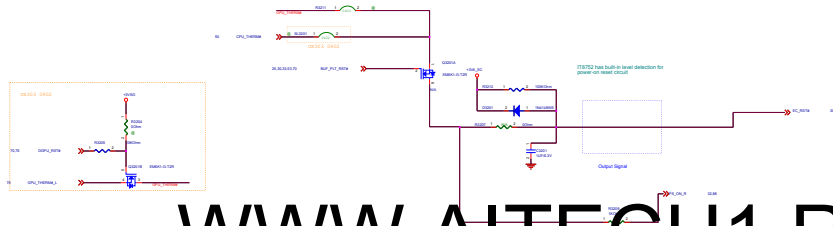
Pin Assignment		
Pin Assignment and Description		
Pin #	Signal	Description
1	VCC	VCC, 5 V, +5V Power supply: 100 mW max.
2	NC	Not connected to the connector for system auto-up
3	NC	Not connected
4	NC	Not connected
5	GND	Ground
6	PC_SDA	I ² C data
7	PC_SCL	I ² C clock
8	INT	Interrupt (low-pulse) line to send data to system (4-wire)



BCA

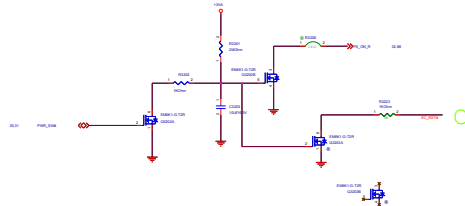
		Project Name X441UBR		Rev 102.1
Title : EC-IT8572(2)_KB,TP				
Size A	Dept.: ASUSTek COMPUTER INC.		Engineer: EE	
Date: Friday, April 27, 2018			Sheet 31	of 102

Thermal Policy

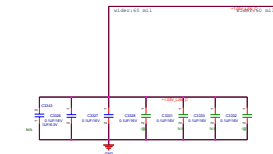


WWW.AITECH1.RU

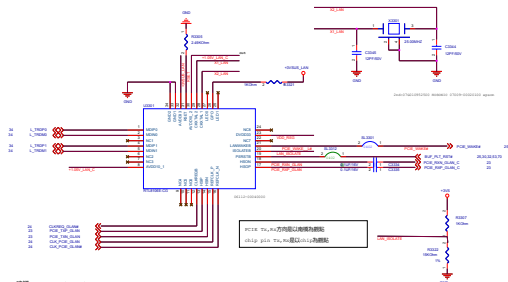
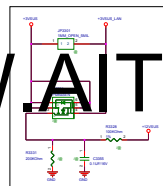
battery embedded (press pwr_sw 10sec, then reset ec)



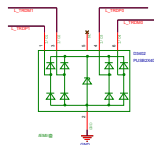
The distance from U3301.34 to L3301 within 200 mil.
The distance from L3301 to +1.05V_LAN_C within 200 mil.



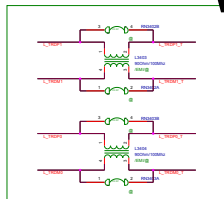
RTS to LAN raise time >0.5ms



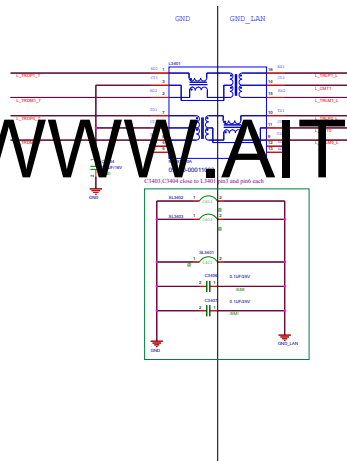
WWW.AITECH1.RU



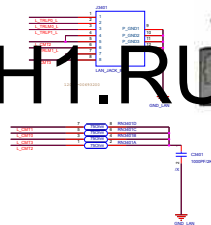
20 L1700P1 <<>
20 L1700P1 <<>
20 L1700P1 <<>
20 L1700P1 <<>



X540SA R2.0 EMI 换到L3401前

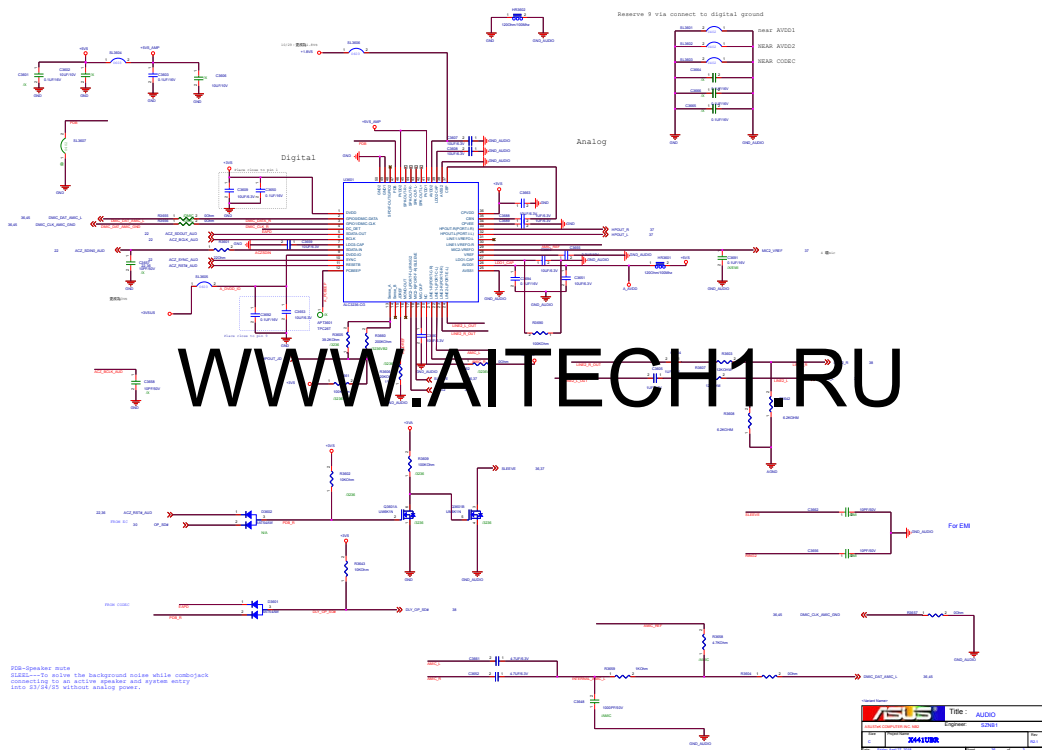


Transformer R2-45
LAN GND

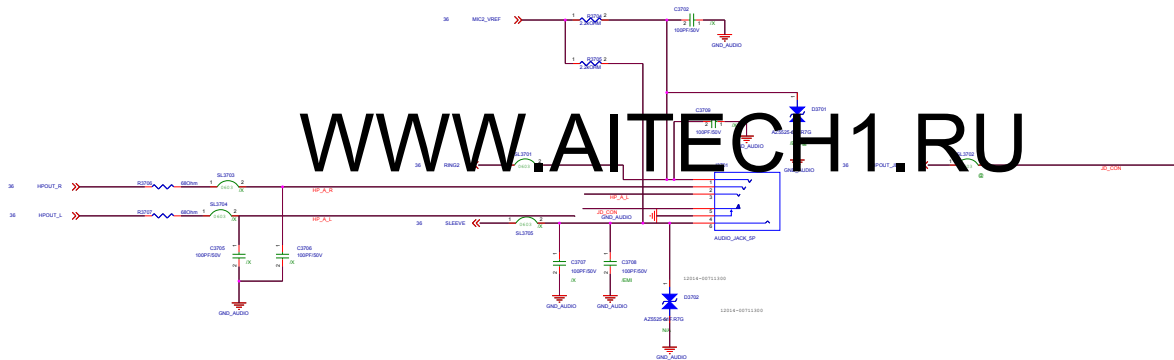


测试点	测试点
1	Test +
2	Test -
3	Test +
4	No Signal
5	No Signal
6	Test -
7	No Signal
8	No Signal

WWW.AITECH1.RU

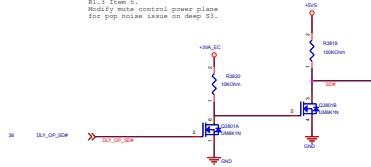


Apple & NOKIA & HP & 4pole MIC

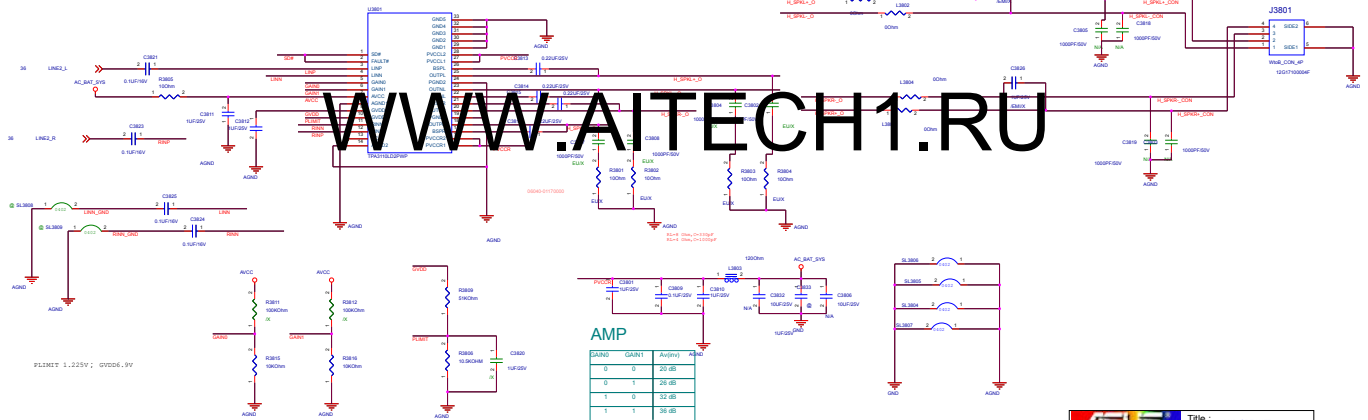


		Title : PHONEJACK	
ASUSTek COMPUTER INC.		Engineer:	
Size Custom	Project Name X441UBR		Rev R2
Date: Friday, April 27, 2018		Sheet	37 of 38

R1.3 item 5.
Modify mute control power plane
for pop noise issue on deep S3.



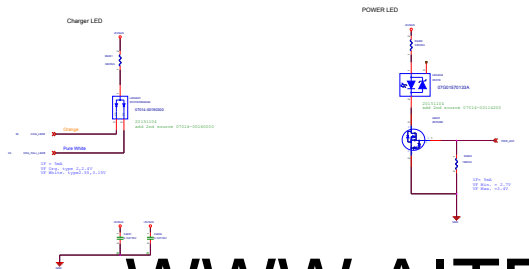
06040-00070100 AUDIO AMP. EUA2313BXIR1



AMP

GAIN0	GAIN1	Av(dB)
0	0	-20 dB
0	1	-20 dB
1	0	-20 dB
1	1	-20 dB

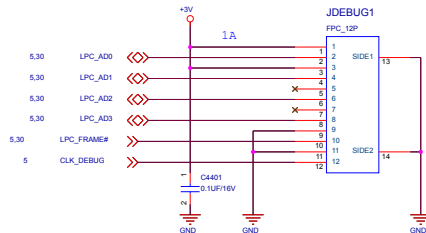
LED indicator 1104 LED 測光



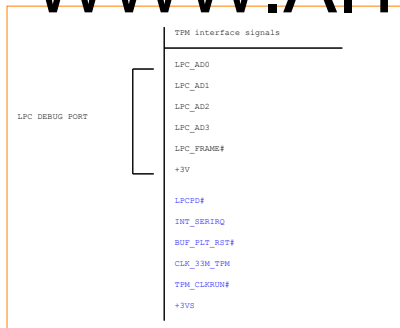
WWW.AITECH1.RU



LPC DEBUG PORT

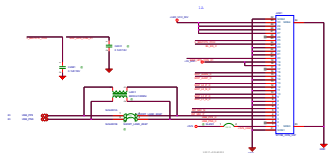
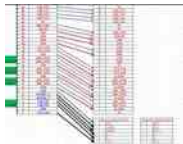


WWW.AITECH1.RU



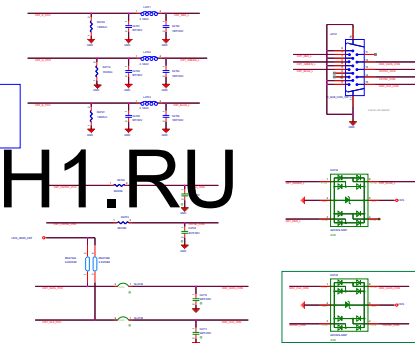
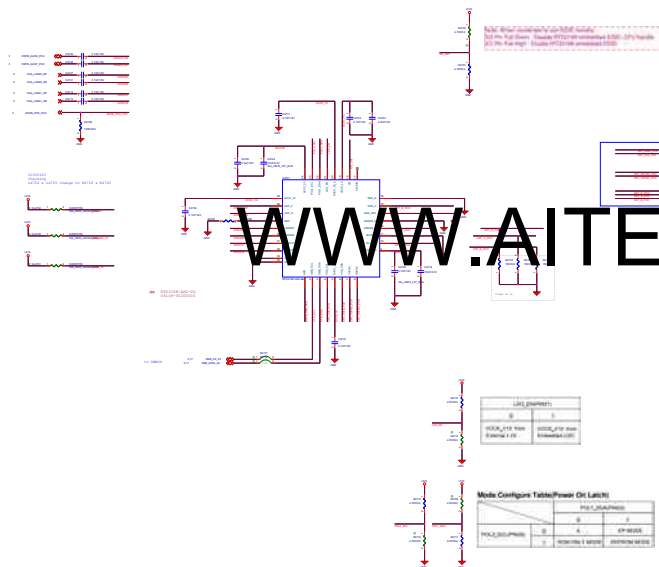
BOM

Project Name		Rev
ASUS X441UBR		R2.1
Title : DEBUG PORT		
Size	Dept. : ASUSTek COMPUTER INC. Engineer: EE	
A	Date: Friday, April 27, 2018	Sheet 44 of 102

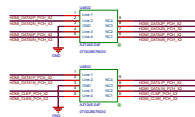
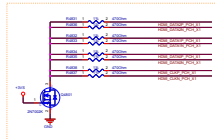
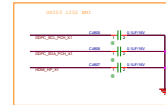
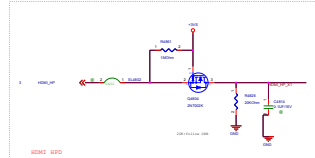


eDP to VGA

CRT D-SUB

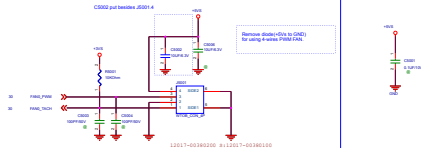


DEAR COM 34801

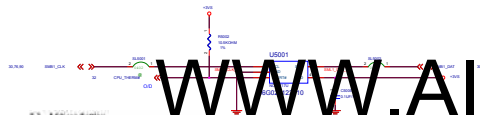


also power down/univers power on: damage pot

PWM Fan



CPU Thermal Sensor



5.3 Address Setting

HEXTTU00000000 address is 00000000 in a 16M bit.

5.6 ALERT pin hardware power-on testing (TED)

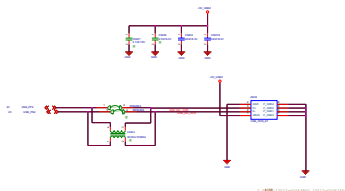
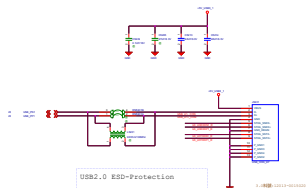
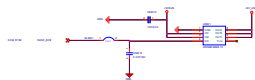
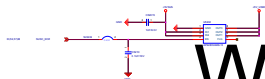
The default value could be set after power up 100ms by different pull-up resistor of ALRT pin.

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	1KΩ	72
	7.5KΩ	90
	10KΩ	100
	15KΩ	110

Route CPU_THRM_DA, CPU_THRM_DC and on the same type
10 mΩ — OTHER SIGNALS
10 mΩ — GND
10 mΩ — (THERM_DA)(10 mΩ)
10 mΩ — (THERM_DC)(10 mΩ)
10 mΩ — GND
10 mΩ — OTHER SIGNALS
Avoid PSB Power

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USB 3.0 con.



WWW.AITECH1.RU

WLAN con.

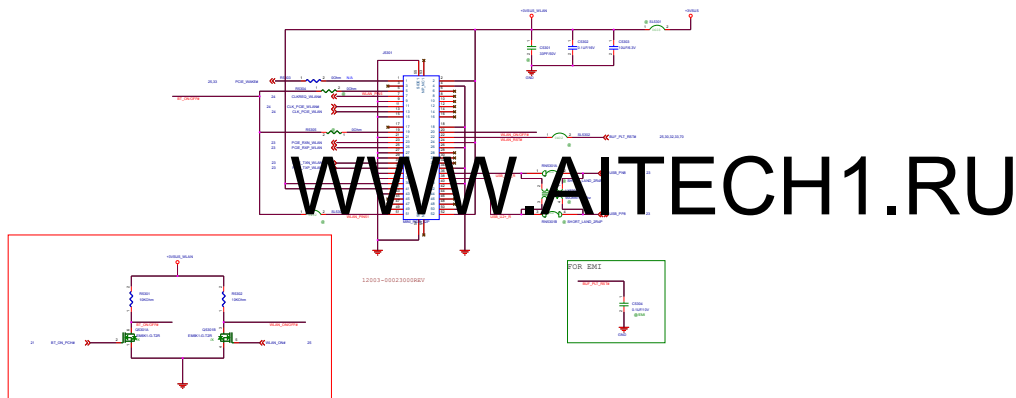
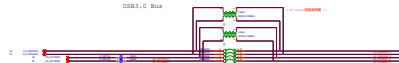


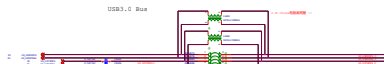
Table 4-1: Pin-to-Pin Mapping for USB Type-C Connector			
Pin No.	Pin Name	Pin No.	Pin Name
1	VBUS	19	NC
2	VBUS	20	NC
3	VBUS	21	NC
4	VBUS	22	NC
5	VBUS	23	NC
6	VBUS	24	NC
7	VBUS	25	NC
8	VBUS	26	NC
9	VBUS	27	NC
10	VBUS	28	NC
11	VBUS	29	NC
12	VBUS	30	NC
13	VBUS	31	NC
14	VBUS	32	NC
15	VBUS	33	NC
16	VBUS	34	NC
17	VBUS	35	NC
18	VBUS	36	NC

Pin No.	Pin Name	Pin No.	Pin Name
1	VBUS	19	NC
2	VBUS	20	NC
3	VBUS	21	NC
4	VBUS	22	NC
5	VBUS	23	NC
6	VBUS	24	NC
7	VBUS	25	NC
8	VBUS	26	NC
9	VBUS	27	NC
10	VBUS	28	NC
11	VBUS	29	NC
12	VBUS	30	NC
13	VBUS	31	NC
14	VBUS	32	NC
15	VBUS	33	NC
16	VBUS	34	NC
17	VBUS	35	NC
18	VBUS	36	NC

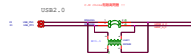
USB3.0 Bus



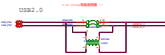
USB3.0 Bus



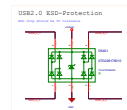
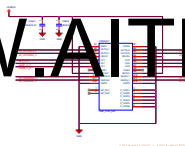
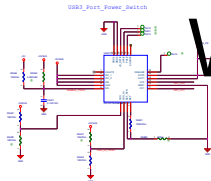
USB2.0



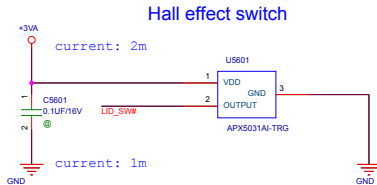
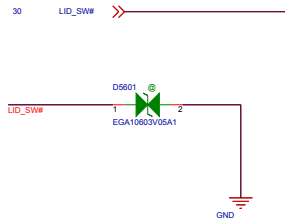
USB2.0



USB1_Port_Power_Switch




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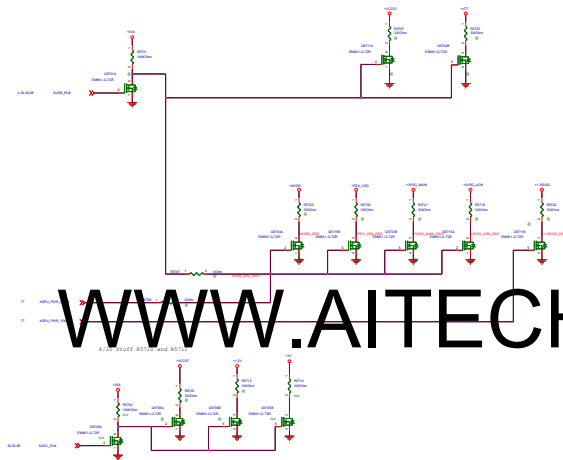


1109:06033-00140000

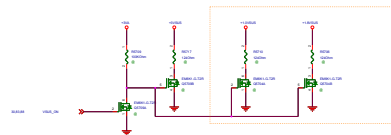
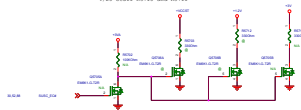
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BOM

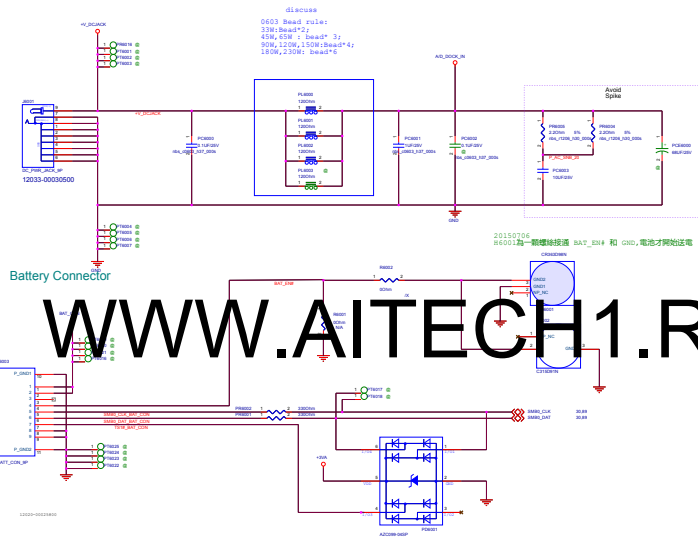
		Project Name	Rev
		X441UBR	R2.1
Title : PWR_SW&HALL_SW			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: EE
A			
Date: Friday, April 27, 2018	Sheet	56	of 102



WWW.AITECH1.RU

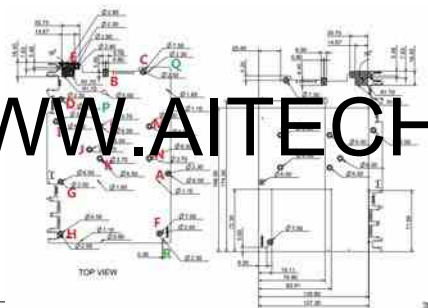
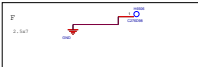
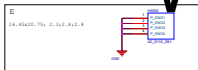
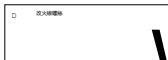






WWW.AITECH1.RU



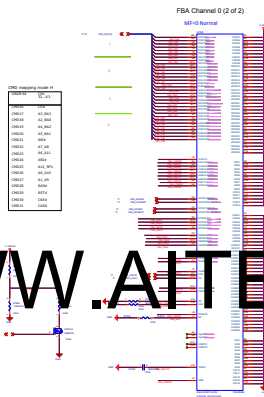
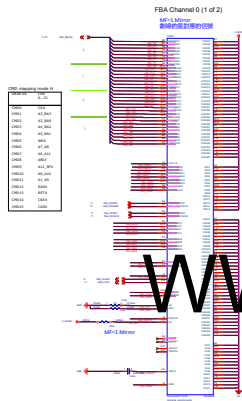
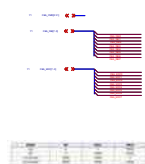




		Project Name		Rev	
		X441URR		R2.1	
Title : N14M_GE_PCIE					
Issd C		Dept: ASUStek COMPUTER INC. Engineer: GE			
Date: Friday, April 21, 2018		Sheet		70	of 100



ASUS		Project Name		Rev	
		X44IUBR		R0.1	
Title : N54M-GE_FB-IF					
Rev		Dept: ASUS TW COMPUTER INC		Engineer: EE	
C					
Date: Friday, April 27, 2018		Sheet		71 of 103	

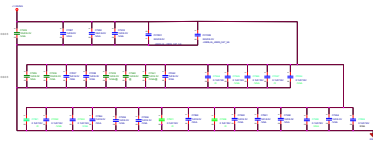


WWW.AITECH1.RU

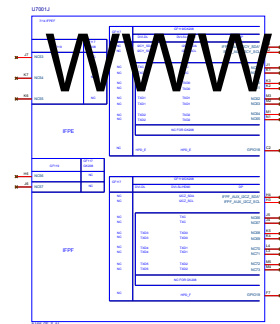
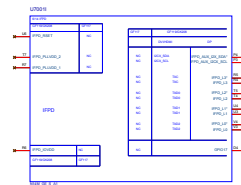
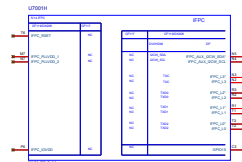
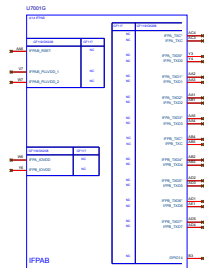
GD5 MODE SELECTION

GD5 MODE SELECTION

GD5 MODE SELECTION



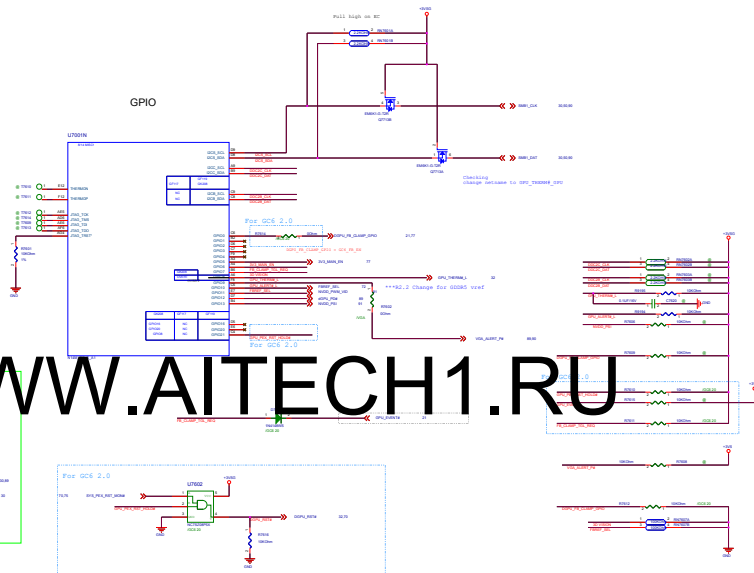
LVDS



CRT

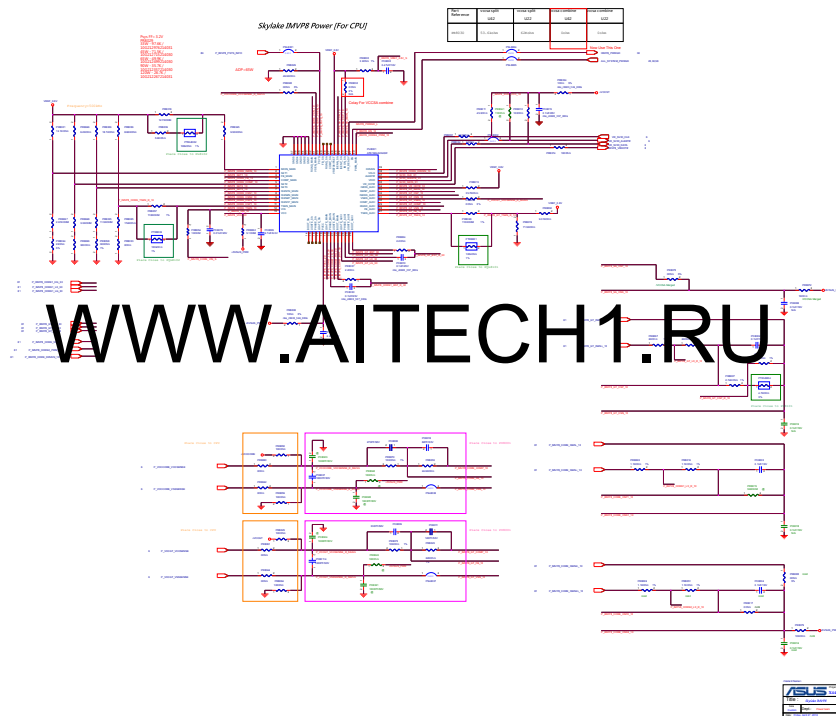


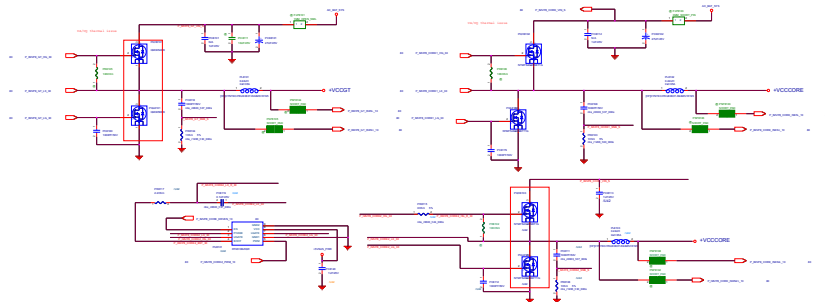
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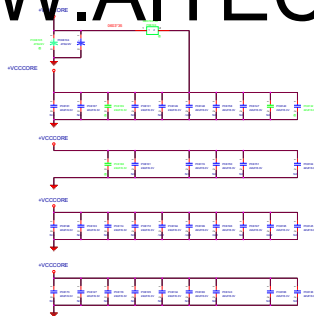
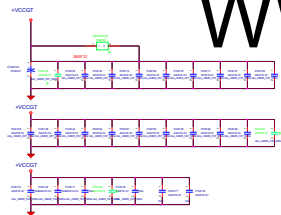
[illegible]

The image contains several circuit diagrams and a schematic. The top diagram shows a differential signal path with components like resistors, capacitors, and a CDR101 clock divider. The middle diagram is a large 'CH1.RU' watermark. The bottom diagram is a detailed schematic of a high-speed signal interface between a GPU and a CPU, featuring a voltage regulator, various control signals, and a high-speed data path.

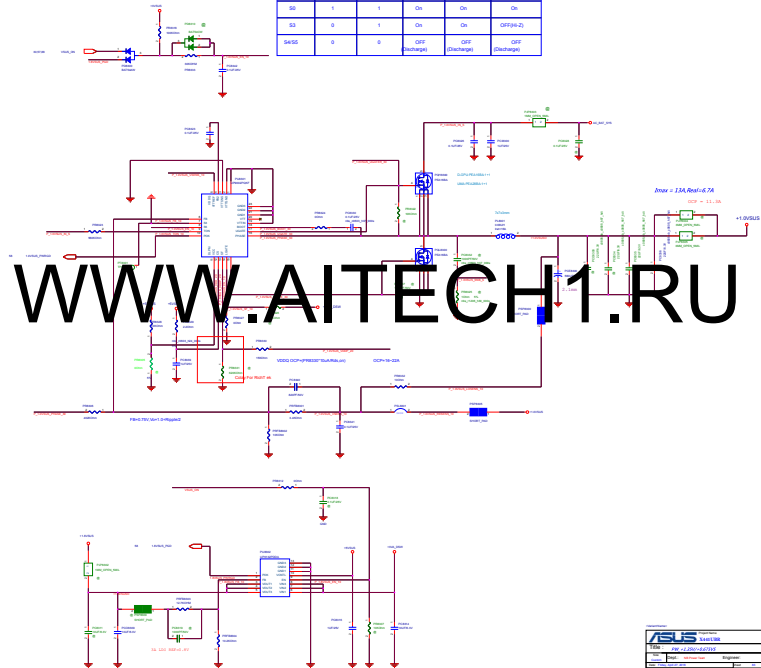




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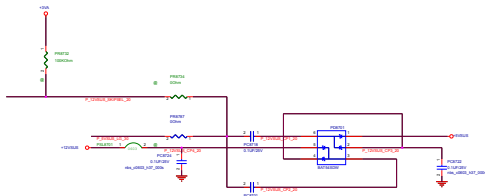
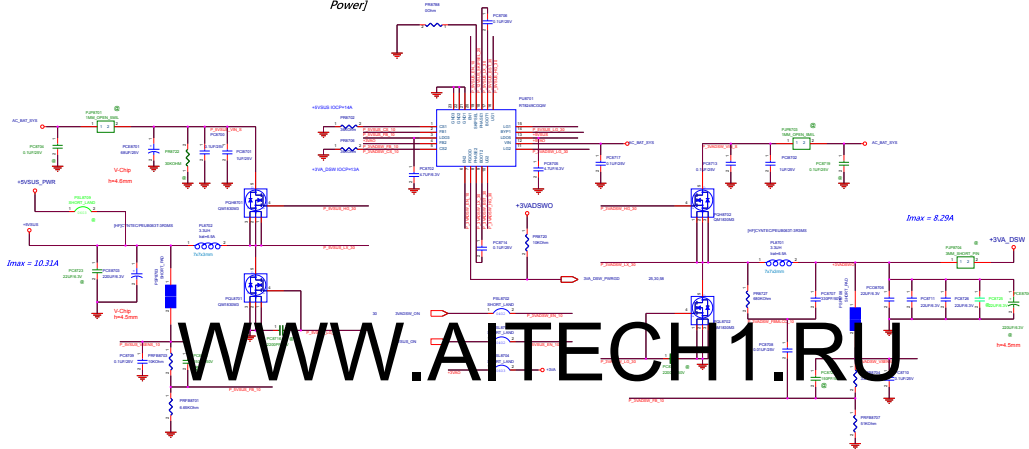


State	Pin7(S3)	Pin8(S6)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(g-z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)





+3VA_DSW /
+5VSUS [System
Power]

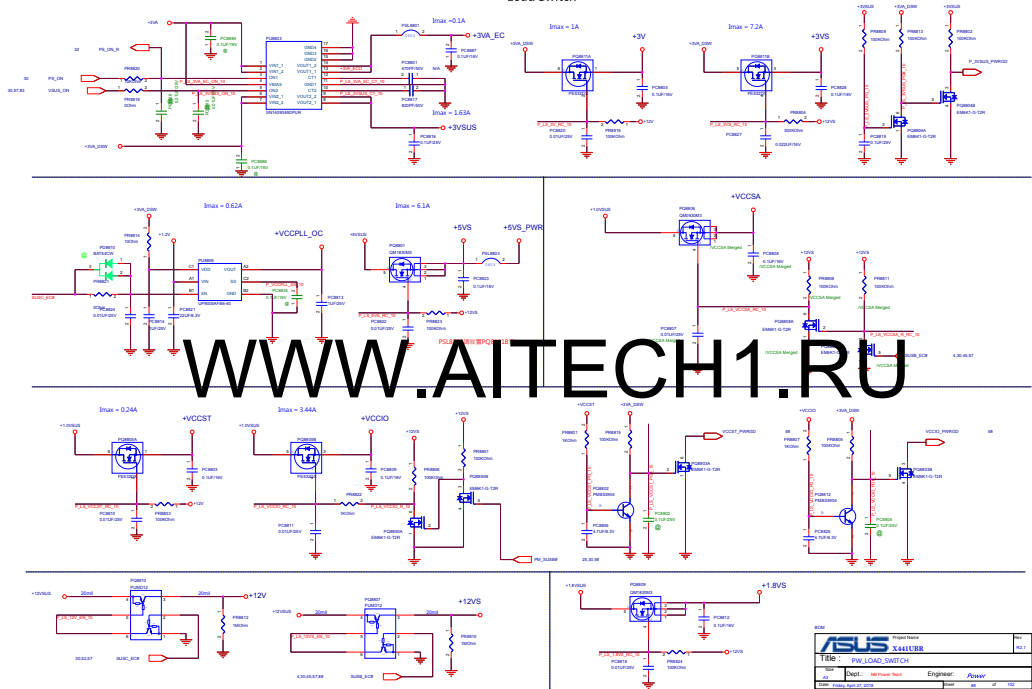


	SR	CR	SR	DR	SR	SR	SR with L20 Change
PS_ON	1	-	-	-	-	-	1
2V50V_ON	1	-	1	-	1	-	1
2V50V_ON	1	-	1	-	0	-	0
3V30V_ON	1	-	1	-	1	-	1
1.8V_ON	1	-	-	-	0	-	0
BLOCK_S0P	1	-	1	-	0	-	0
BLOCK_S0P	1	-	0	-	0	-	0

Battery Mode (MVPB)						
	SS	CS	SS	SS	SS	SS with USB Charger
PS_ON	1	-	-	-	0	1
WAKEUP_ON	1	-	-	1	0	0
WAKEUP_ON	1	-	-	0	0	0
WAKEUP_ON	1	-	-	1	0	1
1.80V_ON	1	-	-	1	0	0
WAKEUP_ON	1	-	-	0	0	0
WAKEUP_ON	1	-	-	0	0	0



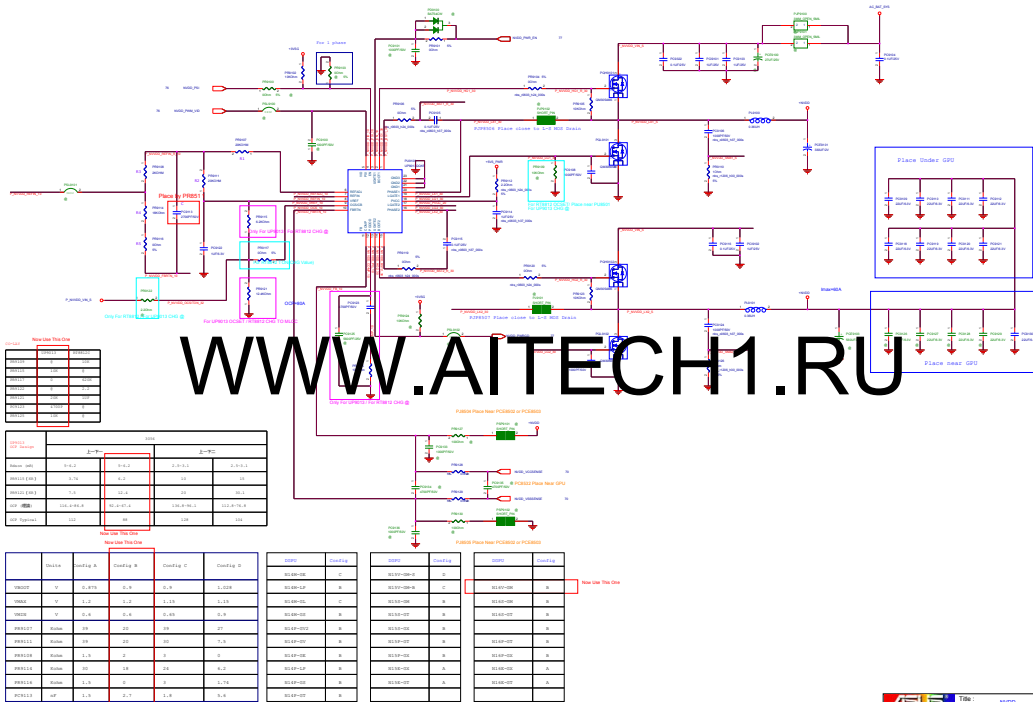
Load Switch

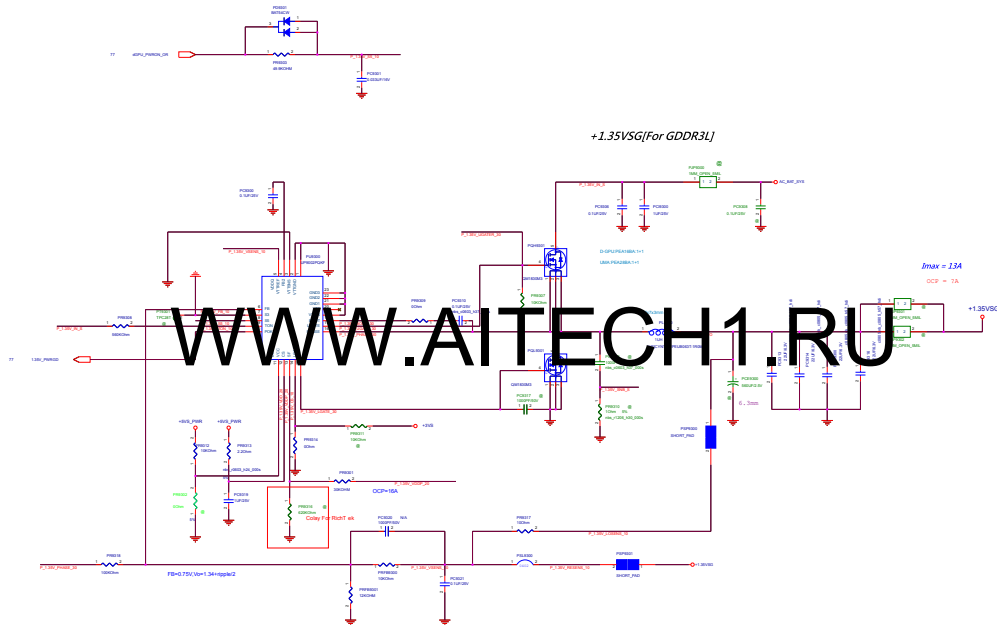


Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Address	Gx00	Gx01	Gx02	Gx03	Gx04	Gx05	Gx06
R/W	M	M	M	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert







Project Name		Rev
ASUS X440UR		Rev 1
Title		PW +1.35V/+0.675V
Author	Dept.	Engineer
Check	Design	Rev

	1	+3VA/+5VA/+3VA/EC	
(EC to EC)	2	EC_RST#	
(EC to power)	3	VSSUS_ON	
		+3VSSUS/+5VSSUS	
(PCB to EC)	4	ME_SSPwrOnAck	
(power to EC)	5	SUS_PWRGD	
(EC to PCB)	6	PM_RST#	
(EC to PCB)	7	AC_PRESENT	
		(to EC)	
(EC to PCB)	8	PM_SW#	
(PCB to EC)	9	PM_RST#IN	
(PCB to EC)	10	PM_SLP_A#	
(PCB to EC)	11	PM_SUSC#	
	12	PM_SUS#/SLP_LAN#	
(PCB to EC)		(PCB to power)	
		+1.1VM_LAN	
(EC to power)		ME_SLP_H_RST#	
		+1.1VM/+3VM	
(EC to power)	13	SUSC_EC#	
		+0.6V/+1.2V/+1.8V/+3V/+5V	
(EC to power)	14	EC_RST#	
		+1.05V/+1.25V/+1.5V/+3V/+5V	
(power to EC)		ME_VM_PWRGD	
(EC to PCB)		ME_PWROK	
	15	SYSTEM_PWRGD	
		+VTT_CPU	
(CPU to power)		GFX_VM_ON	
16	+VTT_CPU_PWRGD/	17	+VTT_PWRGD
		(power to CPU)	
		GFX_VTD	
		+V GFX_CORE	
(power to EC)		GFX_PWRGD	
	18	ALL_SYSTEM_PWRGD	
(EC to power)		CPU_VMON	
	19	+VCCIN	
		(inversion of CLK_2M)	
(power to EC)	20	CORE_PWRGD	
(EC to PCB)	21	PM_PWROK	
(PCB to CPU)		H_DRAMPWRGD	
(PCB to CPU)		H_CPOWRRGD	
(PCB to CPU)	22	BUFF_PLT_RST#	

Timing Diagram Rev.2.1



AC-IN Mode



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